WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor sensor chip, the method comprising:

forming conductor lines on a front surface of a semiconductor wafer in column and row interstices along which a plurality of sensor chips are diced out from the semiconductor wafer;

anisotropically etching predetermined portions of a rear surface of the semiconductor wafer to form a diaphragm for each sensor chip by making a cavity corresponding to the diaphragm;

isotropically etching the cavity by applying an electrical voltage to the semiconductor wafer via the conductor lines; and

separating individual sensor chips by dicing the semiconductor wafer along the conductor lines with a dicing blade having a width wider than a width of the conductor lines.

2. The method of manufacturing a semiconductor sensor chip as in claim 1, the method further comprising:

forming first diffused layers along and underneath the conductor lines, the first diffused layers having an impurity density higher than that of the semiconductor wafer and a width narrower than the width of the dicing blade.

3. The method of manufacturing a semiconductor sensor chip as in claim 2, wherein:

the width of the first diffused layers is narrower than the width of the conductor lines.

4. The method of manufacturing a semiconductor sensor chip as in claim 2, wherein:

the semiconductor wafer includes a P-N junction plane; and

the method further includes a step of forming second diffused layers along and underneath the first diffused layers and along the P-N junction plane by diffusing a same type of impurity as that of the first diffused layer, the second diffused layers having an impurity density higher than that of the semiconductor wafer.

5. The method of manufacturing a semiconductor sensor chip as in claim 4, wherein:

a width of the second diffused layers is wider than the width of the dicing blade.

6. A semiconductor sensor chip comprising:

a semiconductor substrate having a P-N junction plane parallel to front and rear surfaces of the semiconductor substrate;

sensing elements formed on the front surface of the semiconductor substrate;

a diaphragm formed by making a cavity on the rear surface of the semiconductor substrate; and

a diffused layer formed on and along the P-N junction plane and exposed to side surfaces of the semiconductor sensor chip, the diffused layer having an impurity density higher than that of the semiconductor substrate.

7. The semiconductor sensor chip as in claim 6, wherein:

corners of the cavity are rounded.

8. The semiconductor sensor chip as in claim 6, wherein:

the semiconductor sensor chip has a rectangular plane shape; and

the diffused layer is exposed to four sides of the sensor chip.

9. A method of manufacturing a semiconductor sensor chip, the method comprising:

preparing a semiconductor wafer having an upper layer and a lower layer, both layers forming a P-N junction plane therebetween;

forming a plurality of sensor elements on the upper layer, each sensor element being separated from one another

by column and row interstices along which individual sensor chips are to be diced out;

diffusing an impurity in the upper layer to form first diffused layers along the interstices, the first diffused layers having an impurity density higher than that of the upper layer;

diffusing the impurity along the P-N junction plane to form second diffused layers positioned underneath the first diffused layers, the second diffused layers having an impurity density higher than that of the upper layer;

forming conductor lines on the upper layer to cover the first diffused layers;

electrochemically etching portions of the lower layer, by applying an electrical voltage to the lower layer through the conductor lines, the first diffused layers and the second diffused layers, to form diaphragms each positioned underneath each sensor element; and

dicing the semiconductor wafer along the conductor lines with a dicing blade to cutout the semiconductor wafer into individual sensor chips, a width of the dicing blade being wider than a width of the conductor lines so that all of the conductor lines are removed by dicing.